CLAIMS

1. A method of FIR filtering a series of real input values with a series of filter coefficients using a processor, the method comprising the steps of (a) loading each of the input values from memory into the processor, and (b) employing each of the loaded input values in the computation by the processor of more than one filter output value at a time, whereby the amount of data which needs to be transferred between memory and the processor is substantially reduced.

2. A method according to Claim 1, wherein the more than one output values are consecutive.

3. A method according to Claim 1 or 2, wherein a multiply-and-accumulate unit in the processor is used in the computation of one of the output values.

4. A method according to Claim 3, further comprising the steps of (a) feeding one of the loaded filter coefficients into a delay register, and (b) using the output of the delay register as the input to the multiply-and-accumulate unit.

5. A method according to Claims 3 or 4, wherein the output of the multiply-and-accumulate unit is pipelined.

6. A method according to any preceding claim, further comprising the step of multiplying each input value with more than one filter coefficient and adding the result of each multiplication to accumulators corresponding to the more than one output values.

7. A method according to any preceding claim, wherein two output values are

computed at a time.

8. A method according to any preceding claim, further comprising the step of downsampling the input values.

9. A method according to Claim 8 when dependent on Claim 5, wherein at least one further delay register is used.

10. A method according to any of Claims 1 to 7, further comprising the step of upsampling the input values.

11. A method according to Claim 10, wherein the more than one output values computed at a time are separated by a number of samples corresponding to the upsampling factor.

12. A processor for FIR filtering a stream of real input values with a series of coefficients, comprising

a plurality of accumulators corresponding to a plurality of filter output values;

means for loading each of the input values and coefficients from memory;

means for performing simultaneous multiplications of the input value with at least some of the coefficients, and

means for adding the results of the multiplications to the respective accumulators,

wherein each loaded input value is used in the calculation of more than one filter output.

13. A processor for FIR filtering a stream of real input values with a series of coefficients, comprising

at least two pairs of multipliers;

at least one pair of adders, each adder connected to the outputs of one pair of multipliers;

at least one pair of accumulators, each accumulator corresponding to a filter output value and connected to the output of one of the adders; and

at least one delay register connected to the input of one of the multipliers, the delay register being connected to one of the multipliers,

wherein the input values are fed into the multipliers and delay register.

14. A processor comprising

a memory interface;

at least two pairs of multipliers;

at least one pair of adders, each adder connected to the outputs of one pair of multipliers;

at least one pair of accumulators, each accumulator corresponding to a filter output value and connected to the output of one of the adders; and

at least one delay register connected to the input of one of the multipliers, the delay register being connected to one of the multipliers,

wherein the memory interface is adapted to load input samples from memory into the inputs of the multipliers and the input of the delay register and store the output of the accumulators back in memory.

15. A processor according to any of Claims 12 to 14, wherein the output of the accumulators is pipelined.

16. A processor according to any of claims 12-15, further comprising a variable-delay FIFO buffer connected to the input of at least one of the multipliers.

17. A processor according to any of Claims 13 to 16, further comprising a second delay register, and wherein the processor downsamples the input stream.

18. A processor according to any of Claims 12 to 16, wherein the processor upsamples the input stream.

19. A substrate having recorded thereon information in computer readable form for performing any of the methods in Claims 1 to 11.

20. A network adaptor comprising a processor according to any of claims 12 to 18.

21. A computer comprising a processor according to any of claims 12 to 18.

22. A modem comprising a processor according to any of claims 12 to 18.